IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

1 fw

Applicant:

Steven L. Scott et al.

Title:

DECOUPLED STORE ADDRESS AND DATA IN A MULTIPROCESSOR SYSTEM

Docket No.:

1376.697US1

Filed:

August 18, 2003

Examiner:

Unknown

OIPE GO

Serial No.: 10/643,742

Due Date: N/A

Group Art Unit: 2127

MS Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

 \underline{X} A return postcard.

X A Communication Concerning Related Applications (2 pgs.).

X An Information Disclosure Statement (2 pgs.), Form 1449 (4 pgs.), and copies of 45 cited documents.

If not provided for in a separate paper filed herewith, Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

Customer Number 21186

Atty: Thomas F. Brennan

Reg. No. 35,075

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 315 day of May, 2005.

Name

81gnature

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

(GENERAL)

<u>S/N 10/643,742</u> <u>PATENT</u>

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Steven L. Scott et al.

Examiner: Unknown

Serial No.:

10/643,742

Group Art Unit: 2127

Filed:

August 18, 2003

Docket: 1376.697US1

ditle:

DECOUPLED STORE ADDRESS AND DATA IN A MULTIPROCESSOR

SYSTEM

COMMUNICATION CONCERNING RELATED APPLICATIONS

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related applications in the above-identified patent application:

Serial/Patent No. 10/643,586	Filing Date August 18, 2003	Attorney Docket 1376.699US1	Title DECOUPLED VECTOR ARCHITECTURE
10/643,585	August 18, 2003	1376.700US1	LATENCY TOLERANT DISTRIBUTED SHARED MEMORY MULTIPROCESSOR COMPUTER
10/643,754	August 18, 2003	1376.724US1	RELAXED MEMORY CONSISTENCY MODEL
10/643,758	August 18, 2003	1376.729US1	REMOTE TRANSLATION MECHANISM FOR A MULTINODE SYSTEM
10/643,574	August 18, 2003	1376.730US1	INDIRECTLY ADDRESSED VECTOR LOAD-OPERATE-STORE METHOD AND APPARATUS
10/643,727	August 18, 2003	1376.731US1	METHOD AND APPARATUS FOR INDIRECTLY ADDRESSED VECTOR LOAD-ADD-STORE ACROSS MULTI- PROCESSORS

COMMUNICATION CONCERNING RELATED APPLICATIONS

Serial Number: 10/643,742 Filing Date: August 18, 2003

Title: DECOUPLED STORE ADDRESS AND DATA IN A MULTIPROCESSOR SYSTEM

10/643,741

August 18, 2003

1376.733US1

MULTISTREAM PROCESSING MEMORY-AND BARRIER-SYNCHRONIZATION METHOD AND **APPARATUS**

Page 2

Dkt: 1376.697US1

Continuations and divisionals may be later filed on the cases listed above, or cited to the Examiner in any previous Communication Concerning Related Applications. Applicant requests that the Examiner review all continuations and divisionals of the above-listed or previously-cited patent applications before allowing the claims of the present patent application.

Respectfully submitted,

STEVEN L. SCOTT ET AL.

By Applicants' Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

P.O. Box 2938

Minneapolis, MN 55402

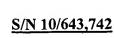
(612) 373-6909

Thomas F. Brennan

Reg. No. 35,075

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 3157 day of May, 2005.

gnature





IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Steven L. Scott et al.

Examiner:

Unknown

Serial No.:

10/643,742

Group Art Unit:

2127

Filed:

August 18, 2003

Docket:

1376.697US1

Title:

DECOUPLED STORE ADDRESS AND DATA IN A MULTIPROCESSOR

SYSTEM

INFORMATION DISCLOSURE STATEMENT

MS Amendment Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 et. seq., the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Several of the attached documents were discovered as a result of a Search Report in Applicants' corresponding foreign patent application. Enclosed for the Examiner's information are a copies of these cited documents and the Search Report.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

Title: DECOUPLED STORE ADDRESS AND DATA IN A MULTIPROCESSOR SYSTEM

Page 2 Dkt: 1376.697US1

Pursuant to 37 C.F.R. 1.98(a)(2), Applicant believes that copies of cited U.S. Patents and Published Applications are no longer required to be provided to the Office. Notification of this change was provided in the United States Patent and Trademark Office OG Notices dated October 12, 2004. Thus, Applicant has not included copies of any US Patents or Published Applications cited with this submission. Should the Office require copies to be provided, Applicant respectfully requests that notice of such requirement be directed to Applicant's below-signed representative. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

STEVEN L. SCOTT ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

P.O. Box 2938

Minneapolis, MN 55402

(612) 373-6909

Date May 31, 2005

Thomas F. Brennar

Reg. No. 35,075

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450,

Alexandria, VA 22313-1450, on this **كاندا** 3 day of May, 2005.

Nama

Signature

PTO/SB/08A(10-01)
Approved for use through 10/31/2002, OMB 851-0031
US Pasent & Trademark Office; U.S. DEPARTMENT OF COMMERCE
Index the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO Complete if Known INFORMATION DISCLOSURE **Application Number** 10/643,742 STATEMENT BY APPLICANT (Use as many shorts as newssary) August 18, 2003 Filing Date Scott, Steven **First Named Inventor Group Art Unit** 2127 **Examiner Name** Unknown Attorney Docket No: 1376.697US1 Sheet 1 of 4

US PATENT DOCUMENTS				
Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Fillng Date If Appropriate
	US- 2004/0044872 A1	03/04/2004	Scott, S. L.	09/04/2002
	US- 2004/0162949 A1	08/19/2004	Scott, S. L., et al.	02/18/2003
	US- 2005/0044340 A1	02/24/2005	Sheets, K. , et al.	08/18/2003
	US-4,771,391	09/13/1988	Blasbalg, Herman	07/21/1986
	US-4,868,818	09/19/1989	Madan, Herb S., et al.	10/29/1987
	US-4,933,933	06/12/1990	Dally, William J., et al.	12/19/1986
	US-5,008,882	04/16/1991	Peterson, , et al.	08/17/1987
	US-5,031,211	07/09/1991	Nagai, Yasuhiro , et al.	02/01/1990
	US-5,036,459	07/30/1991	Den Haan, Petrus A., et al.	03/09/1989
	US-5,105,424	04/14/1992	Flaig, Charles M., et al.	06/02/1988
	US-5,157,692	10/20/1992	Horie, Takeshi, et al.	03/20/1990
	US-5,161,156	11/03/1992	Baum, Richard I., et al.	02/02/1990
	US-5,170,482	12/08/1992	Shu, Renben , et al.	02/13/1991
	US-5,175,733	12/29/1992	Nugent, Steven F.	12/27/1990
	US-5,218,601	06/08/1993	Chujo, Takafumi, et al.	12/20/1990
	US-5,218,676	06/08/1993	Ben-ayed, Mondher, et al.	01/08/1990
	US-5,239,545	08/24/1993	Buchholz, Dale R.	11/05/1990
	US-5,276,899	01/04/1994	Neches, Philip M.	08/10/1990
	US-5,280,474	01/18/1994	Nickolls, John R., et al.	01/05/1990
	US-5,313,628	05/17/1994	Mendelsohn, Noah R., et al.	12/30/1991
	US-5,313,645	05/17/1994	Rolfe, David B.	05/13/1991
	US-5,331,631	07/19/1994	Teraslinna, Kari T.	03/16/1993
	US-5,333,279	07/26/1994	Dunning, Dave	06/01/1992
	US-5,341,504	08/23/1994	Mori, Kinji , et al.	03/01/1990
	US-5,347,450	09/13/1994	Nugent, Steven F.	08/19/1993
	US-5,353,283	10/04/1994	Tsuchiya, Paul F.	05/28/1993
	US-5,365,228	11/15/1994	Childs, Philip L., et al.	08/21/1991
	US-5,434,995	07/18/1995	Oberlin, Steven M., et al.	12/10/1993
	US-5,440,547	08/08/1995	Easki, Hiroshi , et al.	01/05/1994
	US-5,517,497	05/14/1996	LeBoudec, Jean-Yves, et al.	03/21/1995
	US-5,546,549	08/13/1996	Barrett, Linda, et al.	06/01/1994
	US-5,548,639	08/20/1996	Ogura, Takao , et al.	10/22/1992
	US-5,550,589	08/27/1996	Shiojiri, Hiroshisa , et al.	11/04/1994
	US-5,555,542	09/10/1996	Ogura, Takao , et al.	01/11/1996

DATE CONSIDERED EXAMINER

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)	Under the Paperwork Reduction Act of 1996, no persons are required to respond to a collection of information unless it currants a valid time couldn't further. Complete if Known		
	Application Number	10/643,742	
	Filing Date	August 18, 2003	
	First Named Inventor	Scott, Steven	
	Group Art Unit	2127	
	Examiner Name	Unknown	
Sheet 2 of 4	Attorney Docket No: 1376.697US1		

US-6,308,250	10/23/2001	Klausler, P. M.	06/23/1998
US-RE28,577	10/21/1975	Schmidt, William G.	11/21/1973

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	T ²
	EP-0353819A2	02/07/1990	Gupta, Rajiv , et al.	
	EP-0473452A2	03/04/1992	Duerrschmid, O., et al.	
	EP-0475282A2	09/14/1990	Kametani, Masatusugu	
	EP-0501524A2	09/02/1992	Hillis, Daniel W., et al.	
	EP-0570729A2	11/24/1993	Collins, Clive A., et al.	
	WO-87/01750A1	03/26/1987	Anderson, S.	
	WO-88/08652A1	11/03/1988	Hillis, D. W., et al.	
	WO-95/16236A1	06/15/1995	Oberlin, Steven M., et al.	
	WO-96/10283A1	04/04/1996	Bonner, J.	
	WO-96/32681A1	10/17/1996	Thorson, Gregory M., et al.	

	OTHE	R DOCUMENTS NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
		"Deadlock-Free Routing Schemes on Multistage Interconnection Networks", IBM	
		Technical Disclosure Bulletin, 35, (December, 1992),232-233	
		"International Search Report for corresponding PCT Application No.	
		PCT/US2004/026814", (March 10, 2005),V2 pgs.	
		ABTS, D., et al., "So Many States, So Little Time: Verifying Memory Coherence	
		in the Cray X1", Proceedings of the International Parallel and Distributed	
		Processing Symposium (IPDPS' 03), (2003), 11-20	
		ADVE, V. S., et al., "Performance Analysis of Mesh Interconnection Networks	
		with Deterministic Routing", <u>Transactions on Parallel and Distributed Systems</u> ,	
		(March 1994),225-246	
		BOLDING, K., "Non-Uniformities Introduced by Virtual Channel Deadlock	
		Prevention", Technical Report 92-07-07, Department of Computer Science and	
		Engineering, FR-35 University of Washington; Seattle, WA 98195, (July 21,	
	. ,	1992),	
		BOLLA, F R., "A Neural Strategy for Optimal Multiplexing of Circuit and Packet-	
		Switched Traffic", Department of Communications, Computer and Systems	
		Science (DIST), University of Genova, 1324-1330	L
		BOURA, Y M., et al., "Efficient Fully Adaptive Wormhole Routing in n-	
		dimenstional Meshes", <u>IEEE</u> , (1994),589-596	
		BUNDY, A., et al., "Turning Eureka Stepsinto Calculations in Automatic	
		Program", <u>UK IT, (IEE Conf. Pub. 316)</u> , (1991),221-226	_
		CARLILE, B. R., "Algorithms and Design: The CRAP APP Shared-Memory	
		System", COMPCON SPRING '93, San Francisco, CA, (February 22, 1993),312-	
		320	

DATE CONSIDERED **EXAMINER**

PTO/SB/084(10-01)
Approved for use through 10/31/2002. OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE.
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of Information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO Complete if Known INFORMATION DISCLOSURE 10/643,742 **Application Number** STATEMENT BY APPLICANT **Filing Date** August 18, 2003 (Use as many sheets as necessary) Scott, Steven **First Named Inventor Group Art Unit** 2127 Unknown **Examiner Name** Attorney Docket No: 1376.697US1 Sheet 3 of 4

	OTHER	R DOCUMENTS NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No ¹	Include name of the author (In CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
		CHIEN, A. A., et al., "Planar-Adaptive Routing: Low-Cost Adaptive Networks for	
		Multiprocessors", Pro. 19th International Symposium on Computer Architecture,	
		(May 1992),268-277	
		DALLY, W. J., et al., "Deadlock-Free Adaptive Routing in Multicomputer	
		Networks Using Virtual Channels", I.E.E.E. Transactions on Parallel and	
		<u>Distributed Systems, 4(4),</u> (April 1993),466-475	ļ
		DALLY, WILLIAM, et al., "Deadlock-Free Message Routing in Multiprocessor	
		Interconnection Networks", IEEE Transactions on Computers, C-36, (May	1
		1987),547-553	ļ
		DALLY, WILLIAM, "Performance Analysis of k-ary n-cube Interconnection	
		Networks", IEEE Transactions on Computers, 39(6), (June 1990),775-785	
		DALLY, W. J., "Virtual Channel Flow Control", Pro. 17th International	
		Symposium on Computer Architecture, pp. 60-68, May 1990,	<u> </u>
		DUATO, J., "A New Theory of Deadlock-Free Adaptive Routing in Wormhole	
		Networks", I.E.E.E. Transactions on Parallel and Distributed Systems, 4(12),	
		(Dec 1993),1320-1331	ļ
		GALLAGER, ROBERT, "Scale Factors for Distributed Routing Algorithm", NTC	
		<u>'77 Conference Record, 2, at 2-1 through 2-5,</u>	ļ
		GHARACHORLOO, K., "Two Techniques to Enhance the Performance of	1
		Memory Consistency Models", Proceedings of the International Conference on	
		Parallel Processing, (1991),1-10	<u> </u>
		GLASS, C. J., et al., "The Turn Model for Adaptive Routing", Pro. 19th	
		Interanational Symposium on Computer architecture, (May 1992),278-287	<u> </u>
		GRAVANO, L, et al., "Adaptive Deadlock- and Livelock-Free Routing with all	
		Minimal Paths in Torus Networks", <u>IEEE Transactions on Parallel and Distributed</u>	
		<u>Systems, 5(12), (December 1994),1233-1251</u>	ļ
		GUPTA, R., et al., "High speed Synchronization of Processors Using Fuzzy	
		Barriers", International Journakl of Parallel Programming 19 (1990) February,	
		No. 1, New York, US pp 53-73,	-
		HENNESSY, J. L., et al., <u>Computer Architecture – A Quantitative Approach</u> (2 nd Edition, 1996, Morgan Kaufman Publishers), pgs. 39-41	
		ISHIHATA, HIROAKI, et al., "Architecture of Highly Parallel AP1000 Computer",	
		Scripta Technica, Inc., Systems and Computers in Japan 24, No. 7,,(1993),pp.	
		69-76	
		JESSHOPE, C. R., et al., "High Performance Communications in Processor	
		Networks", Proc. 16th International Symposium on Computer Architecture, (May	
		1989),pgs. 150-157	
		KIRKPATRICK, S., et al., "Optimization by Simulated Annealing", SCIENCE,	
- <u>-</u>		May 13, 1993, 220(4599), (May 1983),671-680	

EXAMINER DATE CONSIDERED

PTO/SB/084(10-01)
Approved for use through 10/31/2002, OMB 651-0031
US Patant & Trademak Office: U.S. DEPARTMENT OF COMMERCE
on of information unfess it contains a valid OMB control number.

Substitute for form 1449A/PTO	Under the Paperwork Reduction Act of 1945, no persons are required to respond to a detection of intermation diversity available of Complete if Known		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)	Application Number	10/643,742	
	Filing Date	August 18, 2003	
	First Named Inventor	Scott, Steven	
	Group Art Unit	2127	
	Examiner Name	Unknown	
Sheet 4 of 4	Attorney Docket No: 1	376.697US1	

	OTHE	R DOCUMENTS NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the Item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-Issue number(s), publisher, city and/or country where published.	T ²
		LINDER, D. H., et al., "An Adaptive and Fault Tolerant Wormhole Routing	
		Strategy for k-ary n-cubes", <u>IEEE TRANSACTIONS ON COMPUTERS,40(1)</u> ,	
		(1991),pgs. 2-12	
		LUI, Z. et al., "Grouping Virtual Channels for Deadlock-Free Adaptive Wormhole	
		Routing", PARLE '93 Parallel Parallel Architectures and Languages Europe, 5th	
		International PARLE Conference, Munich, Germanyl, (June 14-17, 1993),254-	
		265	
		NUTH, P., et al., "The J-Machine Network", Proceedings of the International	
		Conference on Computer Design: VLSI in Computers and Processors (ICCD '92)	
		(1992), pgs. 420-423	
		O'KEEFE, M. T., et al., "Static Barrier MIMD: Architecture and Performance	
		Analysis", <u>Journal of Parallel and Distributed Computing No. 2,</u> (March 25,	
		1995),pp. 126-132	
		SHUMAY, M., "Deadlock-Free Packet Networks", <u>Transputer Research and</u>	
		Applications 2, NATUG-2 Proceedings of the Second Conference of the North	
		American Transputer Users Group, (October 18-19, 1989),140-177	
		SNYDER, L., "Introduction to the Configurable, Highly Parallel Computer", <u>IEEE</u> ,	
		(January 1982),pp. 4756	ļ
		TALIA, D., "Message-Routing Systems for Transputer-Based Multicomputer",	
		IEEE Micro, Vol. 13, No. 3, XP000380340, (June 1993),62-72	ļ
		WANG, W., et al., "Trunk Congestion Control in Heterogeneous Circuit Switched	
		Networks", <u>IEEE</u> , (July 1992),pgs. 1156-1161	ļ
		WU, MIN-YOU, et al., "DO and FORALL: Temporal and Spacial Control	
		Structures", Procedings, Third Workshop on Compilers for Parallel Computers,	
		ACPC/TR, July 1992,	
		YANG, C. S., et al., "Performance Evaluation of Multicast Wormhole Routing in	
		2D-Torus Multicomputers", <u>IEEE,</u> (1992),173-178	
		YANTCHEV, J., et al., "Adoptive, low latency, deadlock-free packet routing for	
		networks of processors\", IEEE Proceedings, 136, (May 1989),pp. 178-186	

EXAMINER DATE CONSIDERED